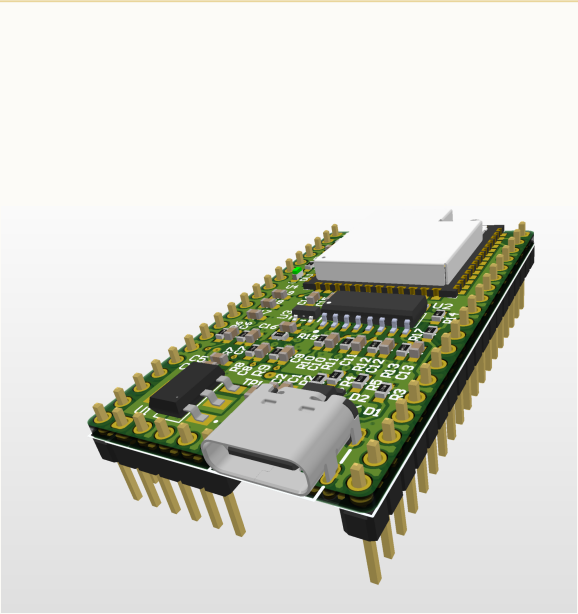
BUILT FOR INNOVATION

Loong Socket ESP32-S3 Module Platform

LS-W1-1119-38P-S3-A00

Compact. Powerful. Connected.
A high-performance ESP32-S3 development platform with native USB-C, external 12-bit ADC and flexible I/O.



MODULE FORMAT

43-contact module
38-pin main dual-row header + 5-pin analog expansion header

ESP32-S3
Dual-core LX7 up to 240 MHz

16 MB Flash
Application and data storage

8 MB PSRAM
Buffers and TinyML workloads

Native USB-C
Power, programming and data

8-ch ADC
MCP3208, 12-bit, 2.500 V VREF

ENGINEERED FOR WHAT'S NEXT

PRODUCT

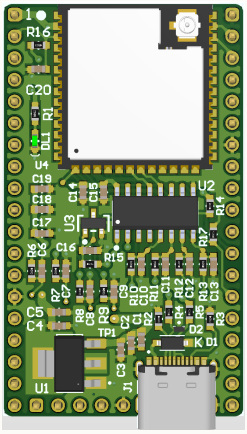
Product Overview

Technical summary and mechanical format

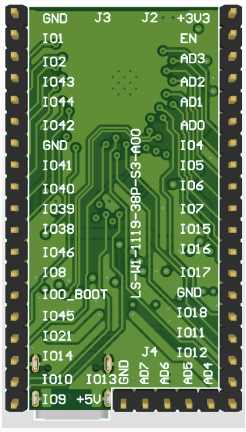
KEY SPECIFICATIONS

Parameter	Value
Module	ESP32-S3-WROOM-1U-N16R8
CPU	Dual-core Xtensa 32-bit LX7 up to 240 MHz
Memory	16 MB Flash + 8 MB PSRAM
Wireless	Wi-Fi 2.4 GHz + Bluetooth Low Energy 5
USB	Native USB-C / USB 2.0 Full Speed
External ADC	MCP3208, 8 channels, 12-bit, SPI
VREF	LM4040A25IDBZR, 2.500 V nominal
Regulator	AZ1117IH-3.3TRG1
USB VBUS diode	1N5819HW-7-F
Module interface	43-contact module
Mechanical interface	38-pin main dual-row header + 5-pin analog expansion header
Approx. PCB size	51.0 mm x 25.4 mm

TOP VIEW



BOTTOM VIEW



INTERFACE DEFINITION

43-contact module

38-pin main dual-row header + 5-pin analog expansion header

The product code keeps **38P** because the 38-pin dual-row header is the main mechanical interface.

38-pin baseboard option

Use only module contacts 1...38. J4 does not need to connect to the carrier PCB.

Full 43-contact option

Connect contacts 1...43 to access ADC4...ADC7 and the extra GND on J4.

Stable numbering

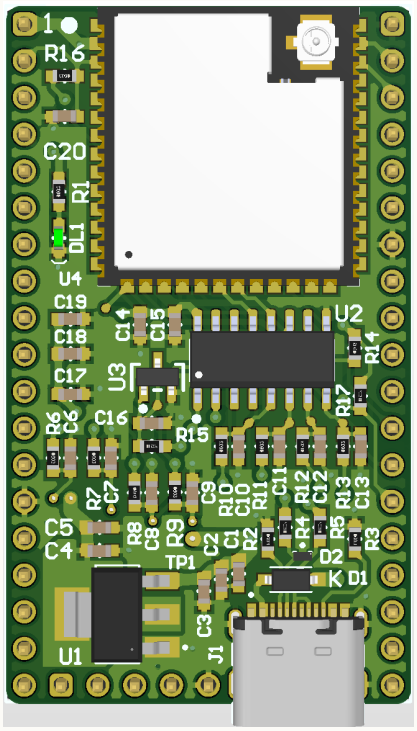
Module contacts 1...38 keep exactly the same global numbers in both connection options.

PRODUCT

Product Views

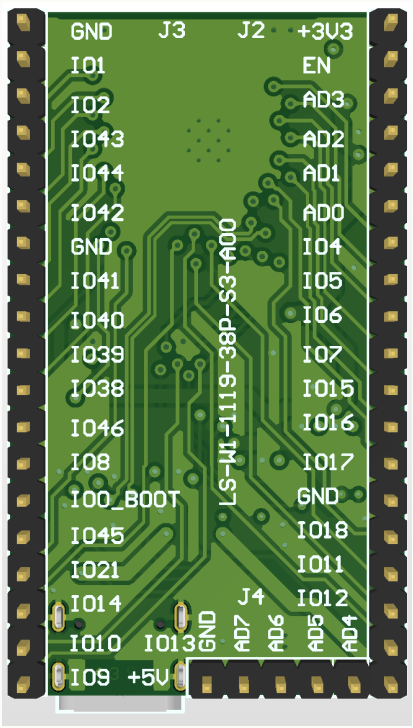
Latest supplied PNG renders - print-friendly presentation

TOP VIEW (FRONT)



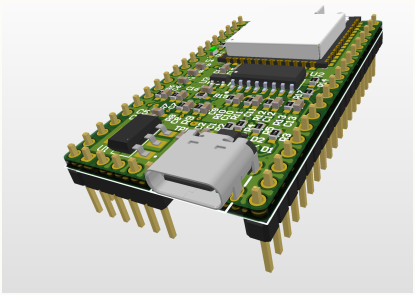
Component side with USB-C and ESP32-S3 module.

BOTTOM VIEW (BACK)



Pin legends and J4 analog expansion header.

PERSPECTIVE VIEW



Latest isometric product render.

BASEBOARD CONNECTION OPTIONS

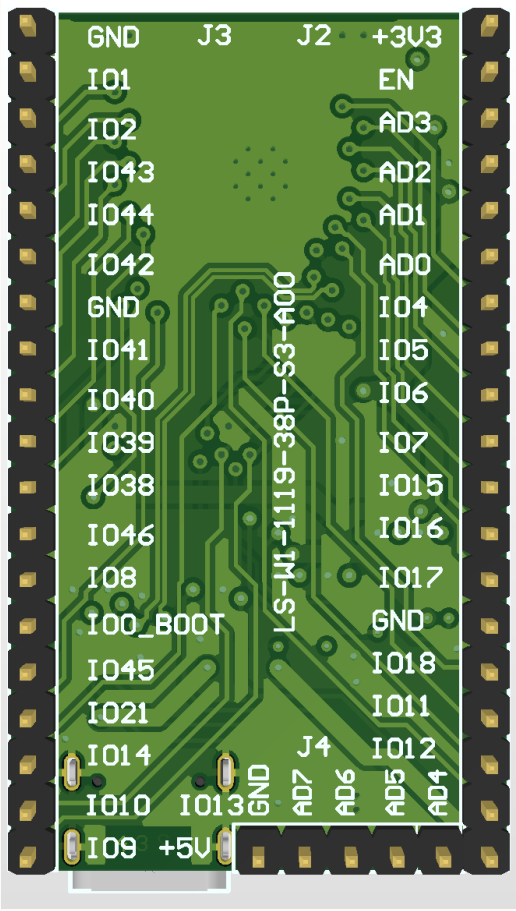
Baseboard use	Connected contacts	Meaning
Main interface only	1...38	Uses the 38-pin main dual-row header. ADC4...ADC7 on J4 are not connected to the carrier PCB.
Full interface	1...43	Uses the full 43-contact module: 38-pin main dual-row header + 5-pin analog expansion header.

INTEGRATION

Pinout Overview

Bottom-view orientation with the USB-C connector pointing downward

BOTTOM VIEW / SILKSCREEN



GLOBAL NUMBERING

Contacts 1...19 follow J2 from top to bottom. Contacts 20...38 follow J3 from bottom to top, so global contact 38 is J3-1. Contacts 39...43 are J4-1...J4-5.

43-CONTACT MODULE

The module has 43 total physical contacts.

MAIN INTERFACE

Contacts 1...38 form the 38-pin main dual-row header.

ANALOG EXPANSION

Contacts 39...43 form the 5-pin J4 analog expansion header: ADC4, ADC5, ADC6, ADC7 and GND.

STRAPPING-RELATED CONTACTS

Module contact 24 = IO45, contact 25 = IO0_BOOT and contact 27 = IO46. Keep external reset-time levels compatible with ESP32-S3 boot requirements.

USB / MEMORY RESERVATIONS

GPIO19 and GPIO20 are reserved for native USB. GPIO35/36/37 are not exposed on the N16R8 variant because of Octal memory usage.

PINOUT

43-Contact Master Pin Assignment

Global module numbering - use this table when a schematic, footprint or harness refers to contacts 1...43.

Pin	Connector	Signal
1	J2-1	+3V3_OUT
2	J2-2	EN
3	J2-3	ADC3
4	J2-4	ADC2
5	J2-5	ADC1
6	J2-6	ADC0
7	J2-7	IO4
8	J2-8	IO5
9	J2-9	IO6
10	J2-10	IO7
11	J2-11	IO15
12	J2-12	IO16
13	J2-13	IO17
14	J2-14	GND
15	J2-15	IO18
16	J2-16	IO11_SPI_MOSI
17	J2-17	IO12_SPI_CLK
18	J2-18	IO13_MISO
19	J2-19	+5V_IN
20	J3-19	IO9_SPI_/CS1/GPIO
21	J3-18	IO10_SPI_/CS2/GPIO
22	J3-17	IO14_SPI_/CS3/GPIO

Pin	Connector	Signal
23	J3-16	IO21
24	**J3-15**	**IO45**
25	**J3-14**	**IO0_BOOT**
26	J3-13	IO8
27	**J3-12**	**IO46**
28	J3-11	IO38
29	J3-10	IO39
30	J3-9	IO40
31	J3-8	IO41
32	J3-7	GND
33	J3-6	IO42
34	J3-5	IO44
35	J3-4	IO43
36	J3-3	IO2
37	J3-2	IO1
38	J3-1	GND
39	J4-1	ADC4
40	J4-2	ADC5
41	J4-3	ADC6
42	J4-4	ADC7
43	J4-5	GND

NUMBERING NOTES

Contacts 24, 25 and 27 are highlighted because IO45, IO0_BOOT and IO46 are strapping-related pins. **Contacts 39...43** are the J4 analog expansion. A carrier PCB may intentionally leave contacts 39...43 unconnected while the module remains a 43-contact module.

PINOUT

Connector J2

J2 uses module contacts 1...19 in the same order.

J2 Pin	Module Pin	Signal	Type	Description
1	1	+3V3_OUT	P	Regulated 3.3 V rail.
2	2	EN	I	ESP32-S3 reset / enable input.
3	3	ADC3	AI	MCP3208 channel 3, 0...2.500 V.
4	4	ADC2	AI	MCP3208 channel 2, 0...2.500 V.
5	5	ADC1	AI	MCP3208 channel 1, 0...2.500 V.
6	6	ADC0	AI	MCP3208 channel 0, 0...2.500 V.
7	7	IO4	I/O	General GPIO.
8	8	IO5	I/O	General GPIO.
9	9	IO6	I/O	Recommended PWM/LEDC output.
10	10	IO7	I/O	Recommended PWM/LEDC output.
11	11	IO15	I/O	General GPIO.
12	12	IO16	I/O	General GPIO.
13	13	IO17	I/O	General GPIO.
14	14	GND	P	Common reference.
15	15	IO18	I/O	General GPIO.
16	16	IO11_SPI_MOSI	I/O	Shared with onboard MCP3208 bus.
17	17	IO12_SPI_CLK	I/O	Shared with onboard MCP3208 bus.
18	18	IO13_MISO	I/O	Shared with onboard MCP3208 bus.
19	19	+5V_IN	P	5 V node; USB VBUS reaches this rail through D1.

PINOUT

Connector J3

J3 connector numbering and global module numbering run in opposite directions: J3-1 = module contact 38, and J3-19 = module contact 20.

J3 Pin	Module Pin	Signal	Type	Description
1	38	GND	P	Common reference.
2	37	IO1	I/O	RTC_GPIO1 / TOUCH1 / ADC1_CH0.
3	36	IO2	I/O	RTC_GPIO2 / TOUCH2 / ADC1_CH1.
4	35	IO43	I/O	UART0 TX / general GPIO.
5	34	IO44	I/O	UART0 RX / general GPIO.
6	33	IO42	I/O	General GPIO.
7	32	GND	P	Common reference.
8	31	IO41	I/O	General GPIO.
9	30	IO40	I/O	General GPIO.
10	29	IO39	I/O	General GPIO.
11	28	IO38	I/O	General GPIO.
12	27	IO46	I/O	Strapping-related. Keep LOW/floating during reset; add baseboard pull-down if needed.
13	26	IO8	I/O	General GPIO.
14	25	IO0_BOOT	I/O	BOOT strapping. Pull LOW during reset for ROM download mode.
15	24	IO45	I/O	Strapping-related pin.
16	23	IO21	I/O	General GPIO.
17	22	IO14_SPI_/CS3/GPIO	I/O	User SPI chip-select or GPIO; add pull-up if active-LOW.
18	21	IO10_SPI_/CS2/GPIO	I/O	User SPI chip-select or GPIO; add pull-up if active-LOW.
19	20	IO9_SPI_/CS1/GPIO	I/O	User SPI chip-select or GPIO; add pull-up if active-LOW.

INTERFACES

Analog Expansion, SPI and Peripherals

J4 - 5-PIN ANALOG EXPANSION

J4 Pin	Module Pin	Signal	Description
1	39	ADC4	MCP3208 channel 4 input, 0...2.500 V.
2	40	ADC5	MCP3208 channel 5 input, 0...2.500 V.
3	41	ADC6	MCP3208 channel 6 input, 0...2.500 V.
4	42	ADC7	MCP3208 channel 7 input, 0...2.500 V.
5	43	GND	Common analog reference.

ADC DESIGN NOTES

The **MCP3208** uses IO3 (/CS, internal), IO11 (MOSI), IO12 (CLK) and IO13 (MISO). The nominal VREF is generated by **LM4040A25IDBZR** at 2.500 V. A local 100 ohm + 1 nF network provides high-frequency damping at each ADC input. For slower industrial or sensor signals, use appropriate input protection, scaling and a lower-frequency external filter.

DIGITAL PERIPHERALS AND ROUTING

Function	Availability / Notes
GPIO Matrix	Most digital peripherals can be routed to free GPIO pins.
UART0 / UART1 / UART2	UART0 is directly available on IO43/IO44; other UART signals are software-routable.
I2C	SDA and SCL may be assigned to free GPIO pins in firmware.
SPI2 / SPI3	General-purpose SPI is available; IO11/IO12/IO13 are wired to the MCP3208.
LEDC PWM	IO6 and IO7 are preferred outputs. IO9/IO10/IO14 are alternatives when not used as SPI chip-select.
MCPWM	Use MCPWM when complementary outputs, motor control or dead-time are required.
USB	GPIO19 = USB D- and GPIO20 = USB D+; reserved for the native USB-C interface.
Unavailable pins	GPIO35/36/37 are not exposed on N16R8 due to Octal memory usage.

PRACTICAL RECOMMENDATIONS

Use **IO6** and **IO7** as first-choice PWM outputs. Keep **IO0_BOOT**, **IO45** and **IO46** free of conflicting reset-time levels. If IO9/IO10/IO14 are used as active-LOW SPI chip-select signals, add pull-up resistors on the carrier PCB.

PRODUCT

Power, USB and Ordering Information

POWER ARCHITECTURE

5 V may be applied through USB-C or **+5V_IN**. USB VBUS reaches the 5 V rail through **1N5819HW-7-F**. The local 3.3 V domain is generated by **AZ1117IH-3.3TRG1**. GPIO are 3.3 V only and are not 5 V tolerant.

USB / PROGRAMMING

Native USB supports power, flashing, USB-CDC and USB Serial/JTAG. UART0 remains available on IO43/IO44. USB reconnection restarts host enumeration but does not replace physical access to EN/IO0_BOOT if firmware leaves native USB unusable.

ORDERING / IDENTIFICATION

Item	Code / Note
PCB	LS-W1-1119-38P-S3-A00
Assembled variant	LS-W1-1119-38P-S3U-N16R8-V2500-A00
Datasheet	DS_LS-W1-1119-38P-S3-A00_A07
Main module	ESP32-S3-WROOM-1U-N16R8
VREF	V2500 = LM4040A25IDBZR, 2.500 V nominal
LDO	AZ1117IH-3.3TRG1
USB diode	1N5819HW-7-F

VALIDATION CHECKLIST

Before final release, validate USB enumeration/recovery, voltage drop under RF peaks, LDO temperature, ADC noise and accuracy, strapping behavior, antenna performance, SPI integrity, ESD and EMC performance of the complete assembly.

REVISION NOTE

A07 / 18-08-2026 - adds the global 1...43 module-contact numbering, documents the two carrier-PCB connection options, and standardizes the wording to **43-contact module** and **38-pin main dual-row header + 5-pin analog expansion header**. Also reviewed the print layout to remove overlaps or stray elements next to text and images.

LOONG SOCKET | ENGINEERED FOR WHAT'S NEXT